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EXAMINER	
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ART UNIT	**PAPER NUMBER**
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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/769,127
Filing Date: January 30, 2004
Appellant(s): MEI, PING

Hewlett-Packard Development Company
Wendell J. Jones
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 06/10/2008 appealing from the Office action mailed 03/13/08.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) **Related Appeals and Interferences**

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5,877,076	Dai	3-1999
6,861,365	Taussig et al	3-2005
2007/0184251	CHIKAGAWA	8-2007

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Dai (U.S. 5,877,076).

As to claim 1, Dai discloses in figures 3i-3k a method for forming a semiconductor device comprising: forming a 3-dimensional pattern (see 161' and 151' in figure 3i) in a substrate (110); and depositing at least one material (180) over the substrate (110) in accordance with desired characteristics of the semiconductor device. It should be noted that: elements 161' and 151' inherently create a 3-dimensional pattern in a substrate so that the material 180 can be deposited within a 3-dimensional pattern.

As to claim 13, Dai discloses in figures 3i-3k a system for forming a semiconductor device comprising: means for forming a pattern (see 161' and 151' in figure 3i) in a substrate (110) wherein the pattern is 3-dimensional; and means for depositing at least one semiconductor material (180) over the substrate (410) in accordance with desired characteristics of the semiconductor device.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 3, 14 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dai (U.S. 5,877,076) in view of Taussig et al (U.S. 6,861,365).

As to claims 3, 14, and 17, Dai does not disclose the semiconductor device comprises a cross-point memory array or at least one of a transistor, a resistor, a capacitor, a diode, a fuse and an anti-fuse.

Taussig et al discloses in figures 1, 2a-2b, and 4a-5 a method for forming a semiconductor device, wherein the semiconductor device comprises a cross-point memory array (see col. 3, lines 61-67); or at least one of a transistor, a resistor, a capacitor, a diode, a fuse and an anti-fuse (see claim 8 and col. 4, lines 14-20). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus of Dai by having a semiconductor device which comprises a cross-point memory array or at least one of a transistor, a resistor, a capacitor, a diode, a fuse and an anti-fuse as taught by Taussig et al for the purpose of intended use, and/or providing different functionality/application by using the different type of chip(s) in the semiconductor device(s)

Allowable Subject Matter

5. Claims 2, 4-10, 15-16, 18-20, and 22-23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

(10) Response to Argument:

- ***Response to argument directed to the rejection of claims 1 and 13 as being anticipated by Dai (U.S. 5,877,076).***

The Appellant argued that Dai's reference does not disclose a 3-dimensional (3D) pattern is formed in a substrate, specifically the pattern(s) 161', 151' are not formed in the substrate (110).

The Appellant's argument has been fully considered but it is not persuasive because Dai's reference clearly discloses in figures 3i-3k a method and a corresponding apparatus comprising a 3-dimensional (3D) pattern (as indicated at 161' and 151') is formed in a substrate {a substrate comprises layers (160, 150, 140, 130, 120 &110) or (140, 130, 120 & 110)}. Thus, the 3-dimensional (3D) pattern(s) created by 161' and 151' in figures 3i-3k of Dai is in the substrate {comprising (160, 150, 140, 130, 120 &110) or (140, 130, 120 & 110)}.

Appellant should note that: a substrate can be a multi-layer substrate, it can comprise more than one layer, and Dai's reference clearly discloses that a substrate comprising layers (160, 150, 140, 130, 120 &110) or (140, 130, 120 & 110). Therefore, the 3-dimensional (3D) pattern(s) created by 161' and 151' are formed in the substrate (see figures 3i-3k in Dai).

For better understanding about a substrate that can be a multi-layer substrate or a substrate that comprises more than one layer, CHIKAGAWA (U.S. 2007/0184251) clearly discloses in figure 1A, a substrate ("a ceramic multilayer substrate" 10) comprises more than one layer.

Since the structure of Dai clearly discloses the same structure as the claimed invention, and thus Appellant's argument is not persuasive.

- ***Response to argument directed to the rejection of claims 3, 14 and 17 as being unpatentable over Dai (U.S. 5,877,076) and Taussig et al (U.S. 6,861,365).***

Appellant further argued that the combined references of Dai and Taussig et al does not make the modification obvious.

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Dai's reference clearly discloses in figures 3i-3k a method and a corresponding apparatus comprising all the limitations, except for a cross-point memory array; or at least one of a transistor, a resistor, a capacitor, a diode, a fuse and an anti-fuse. However, Taussig et al clearly discloses in figures 1, 2a-2b, and 4a-5 a method and a corresponding apparatus for forming a semiconductor device, wherein the semiconductor device comprises a cross-point memory array (see col. 3, lines 61-67); or at least one of a transistor, a resistor, a capacitor, a diode, a fuse and an anti-fuse (see claim 8 and col. 4, lines 14-20). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus of Dai by having a semiconductor device which comprises a cross-point memory array; or at least one of a transistor, a resistor, a capacitor, a diode, a fuse and an anti-fuse as taught by Taussig et al for the purpose of intended used and/or providing different functionality/application by using the different type of chip(s) in the semiconductor device(s).

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejection(s) should be sustained.

Respectfully submitted,

Thanh Tran, Examiner

/T.Y.T./

Sept. 24th 2008

Conferees:

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